



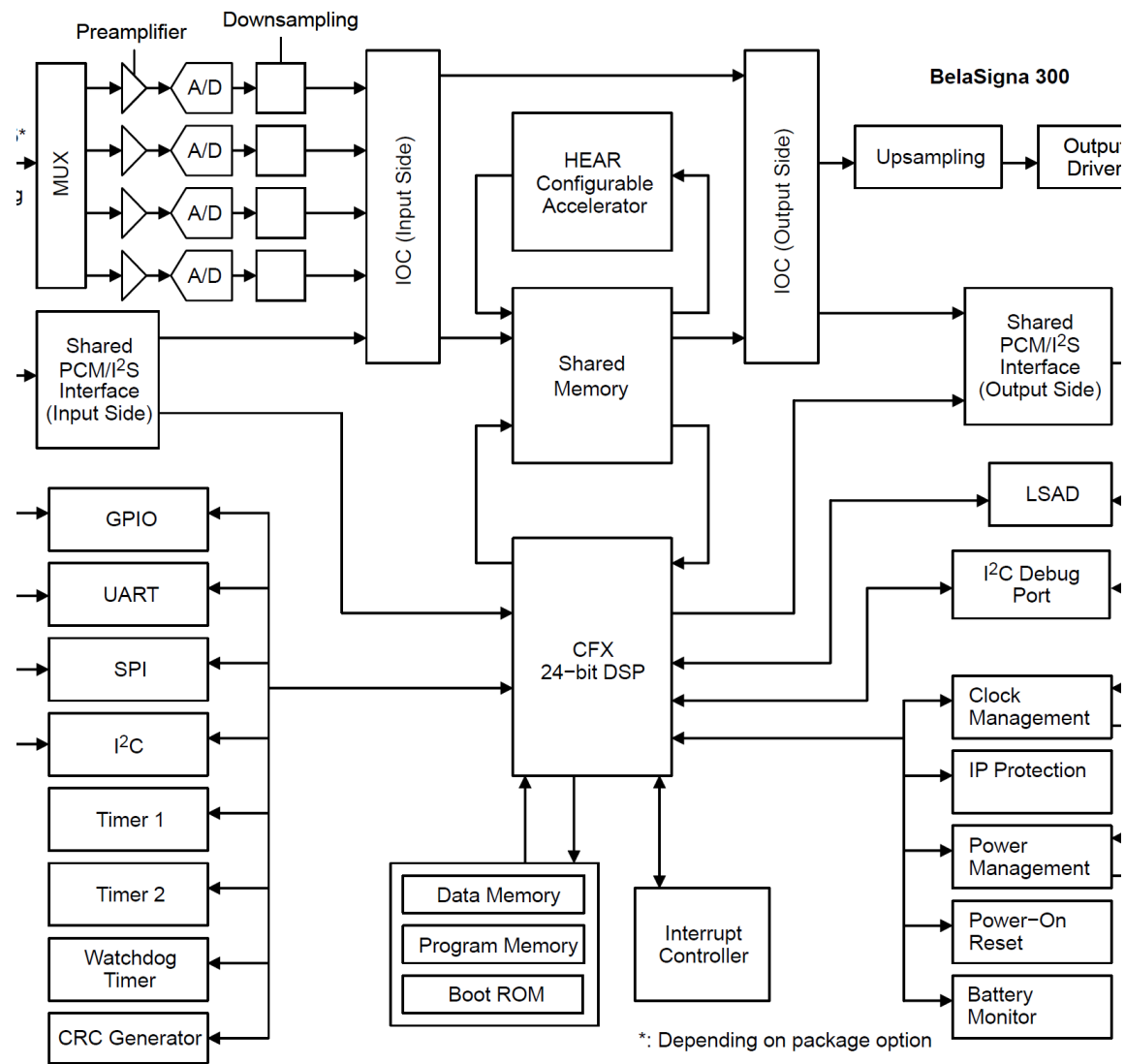
BelaSigna[®]300

助听器算法设计与思路



硬件系统构架

- BelaSigna®300是基于开放构架DSP的混合信号音频处理器。
- 高度灵活可配置的CFX DSP core具有双哈佛结构的24位定点DSP，双发射指令单元，高效的流水线构架
- 专为高效音频算法优化的HEAR加速器，可为多种基础运算提供加速运算
- 灵活的IOC控制器，具有为多通道输入和方向性处理优化的硬件采样延迟配置



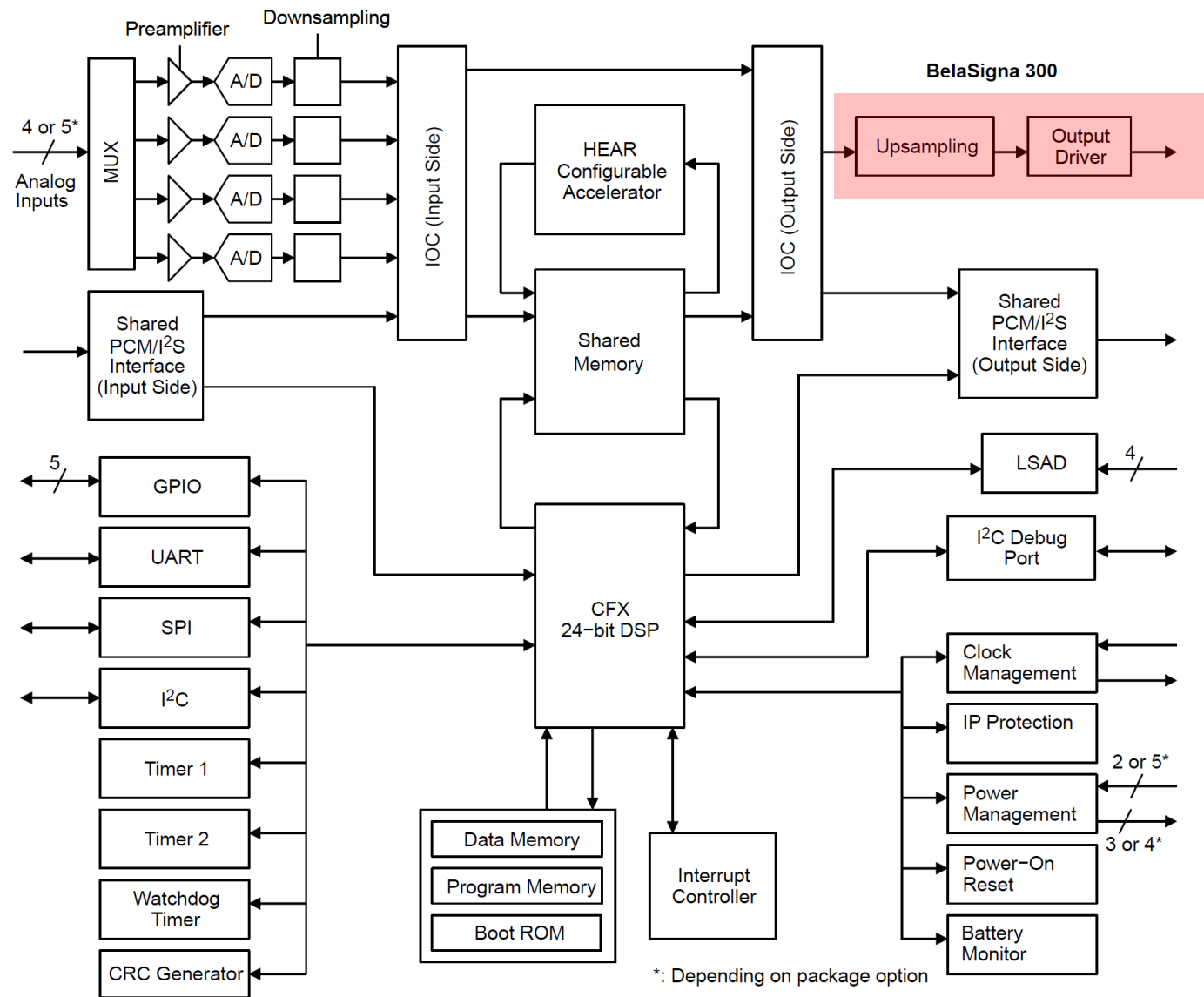
- 配置MUX

- 配置A/D

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- The diagram illustrates the BELA300 SoC architecture, which is centered around a **CFX 24-bit DSP**. The architecture is divided into several functional blocks:
- Input Section (Left):**
 - Analog Inputs:** 4 or 5* inputs are multiplexed (MUX) and then pass through a **Preamplifier** and **A/D** converters before being sampled by **Downsampling** blocks. These feed into the **IOC (Input Side)**.
 - Shared PCM/I²S Interface (Input Side):** Receives external digital audio inputs and feeds into the **IOC (Input Side)**.
 - Core Processing (Center):**
 - The **CFX 24-bit DSP** is the central processing unit, connected to **Shared Memory**, **HEAR Configurable Accelerator**, **Interrupt Controller**, and **Program Memory**.
 - Shared Memory** is connected to the DSP, the **IOC (Output Side)**, and the **Shared PCM/I²S Interface (Output Side)**.
 - HEAR Configurable Accelerator** is connected to the DSP and the **IOC (Output Side)**.
 - Output Section (Right):**
 - The **IOC (Output Side)** feeds into the **Upsampling** block, which then connects to the **Output Driver**.
 - The **Shared PCM/I²S Interface (Output Side)** provides digital audio outputs.
 - LSAD** (Low-Speed Analog-to-Digital) is connected to the DSP and provides a 4-bit output.
 - I²C Debug Port** is connected to the DSP for debugging.
 - Peripheral and Control Blocks (Bottom):**
 - GPIO** (General Purpose Input/Output) with 5 pins.
 - UART** (Universal Asynchronous Receiver/Transmitter).
 - SPI** (Serial Peripheral Interface).
 - I²C** (Inter-Integrated Circuit).
 - Timer 1** and **Timer 2**.
 - Watchdog Timer**.
 - CRC Generator**.
 - Program Memory** and **Boot ROM** are part of the core memory structure.
 - Interrupt Controller** manages system interrupts.
 - Clock Management**, **IP Protection**, **Power Management** (with 2 or 5* pins), **Power-On Reset** (with 3 or 4* pins), and **Battery Monitor** are part of the system control and power management blocks.
- *: Depending on package option

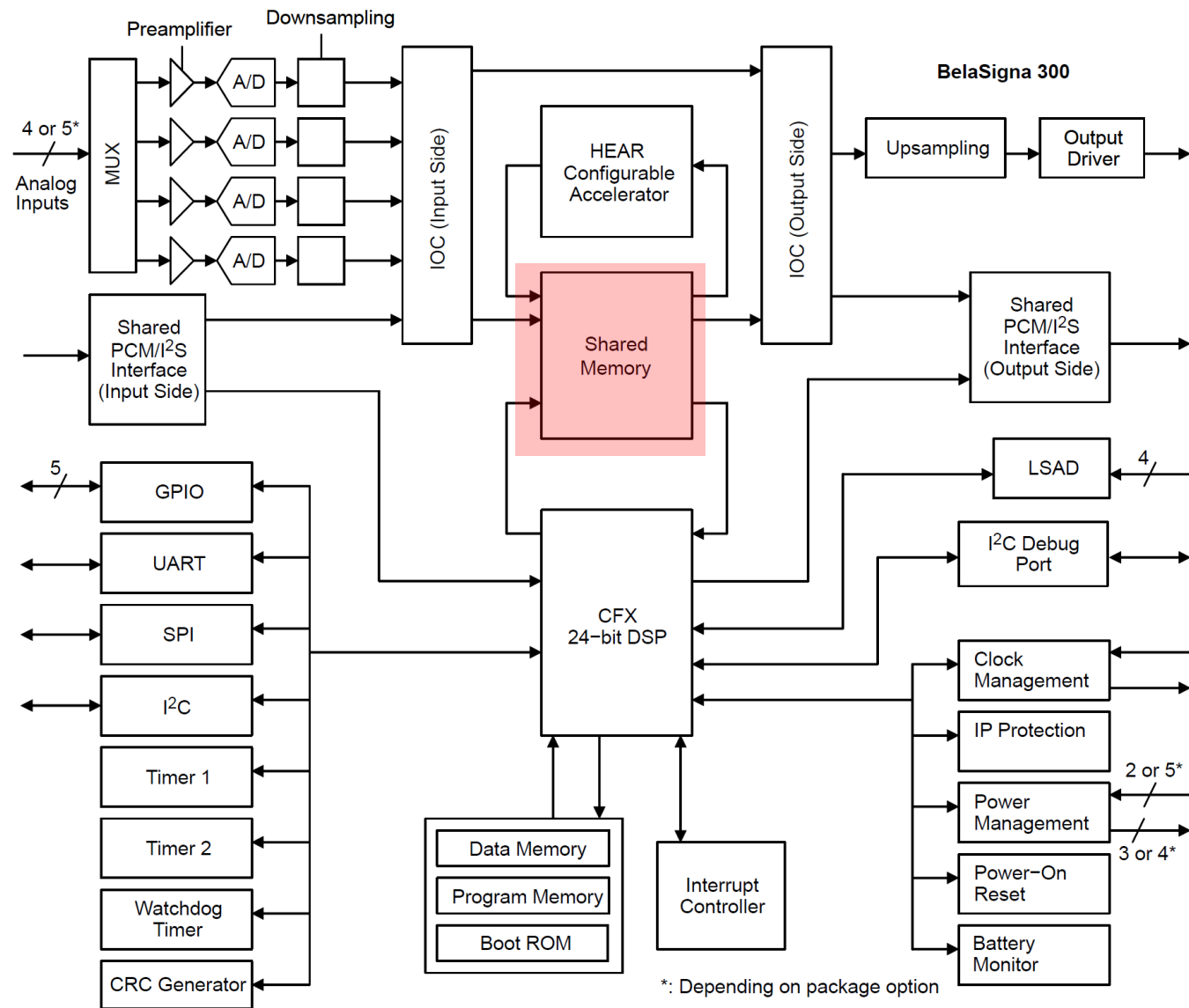
输出部分

- 静音开关接口
- 输出检查



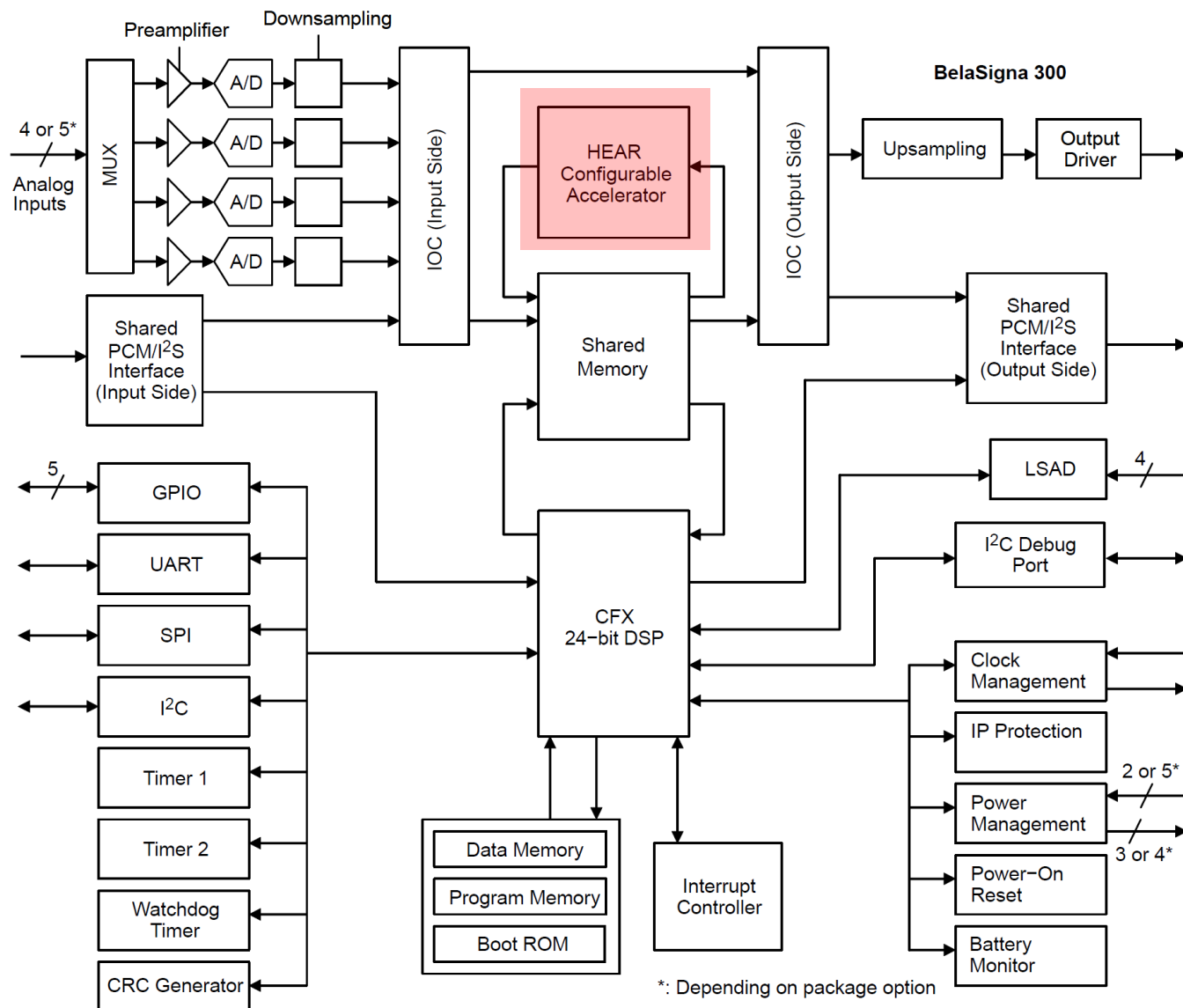
共享内存

- 配置各种FIFO缓存
- 配置HEAR模块内存



HEAR加速器

- 傅里叶模块WOLA Filterbank
 - 信号分解Analysis
 - 应用增益Gain apply
 - 信号合成Synthesis
- 统计模块Signal Statistic
 - 子带能量计算Energy
 - 平均能量与总能量Mean、Sum
 - 信号方差Variance
- 滤波Filter
 - FIR
 - IIR





助听器应用的主要算法模块

灵活可配置的多通道压缩系统

基于长时间言语频谱的语音增强算法

基于短时频谱分析的环境噪音抑制算法

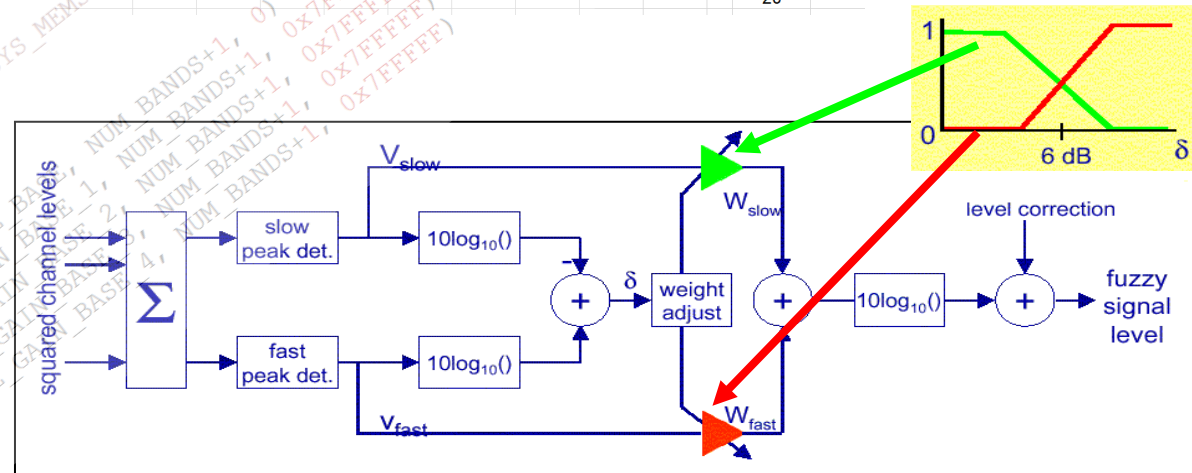
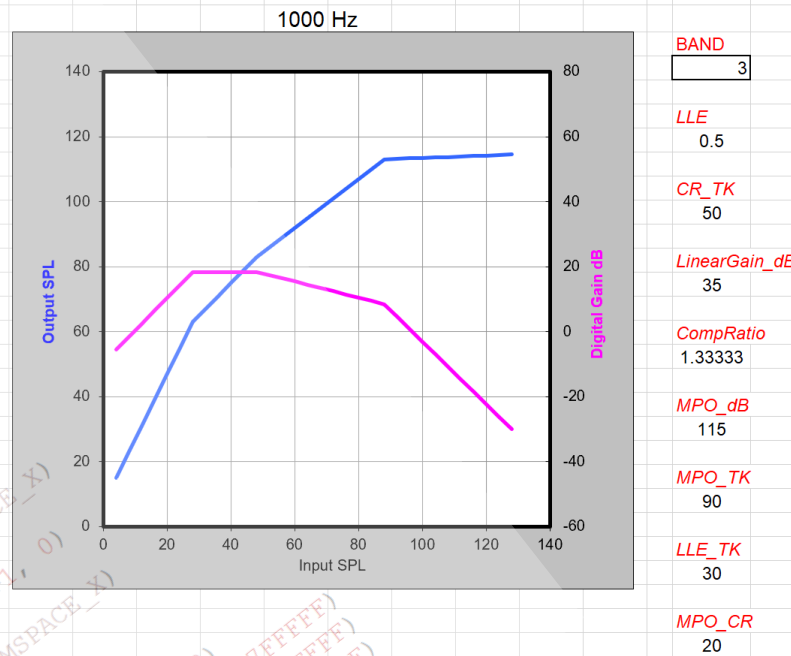
通道反馈侦测及抑制处理

方向性处理

其它功能

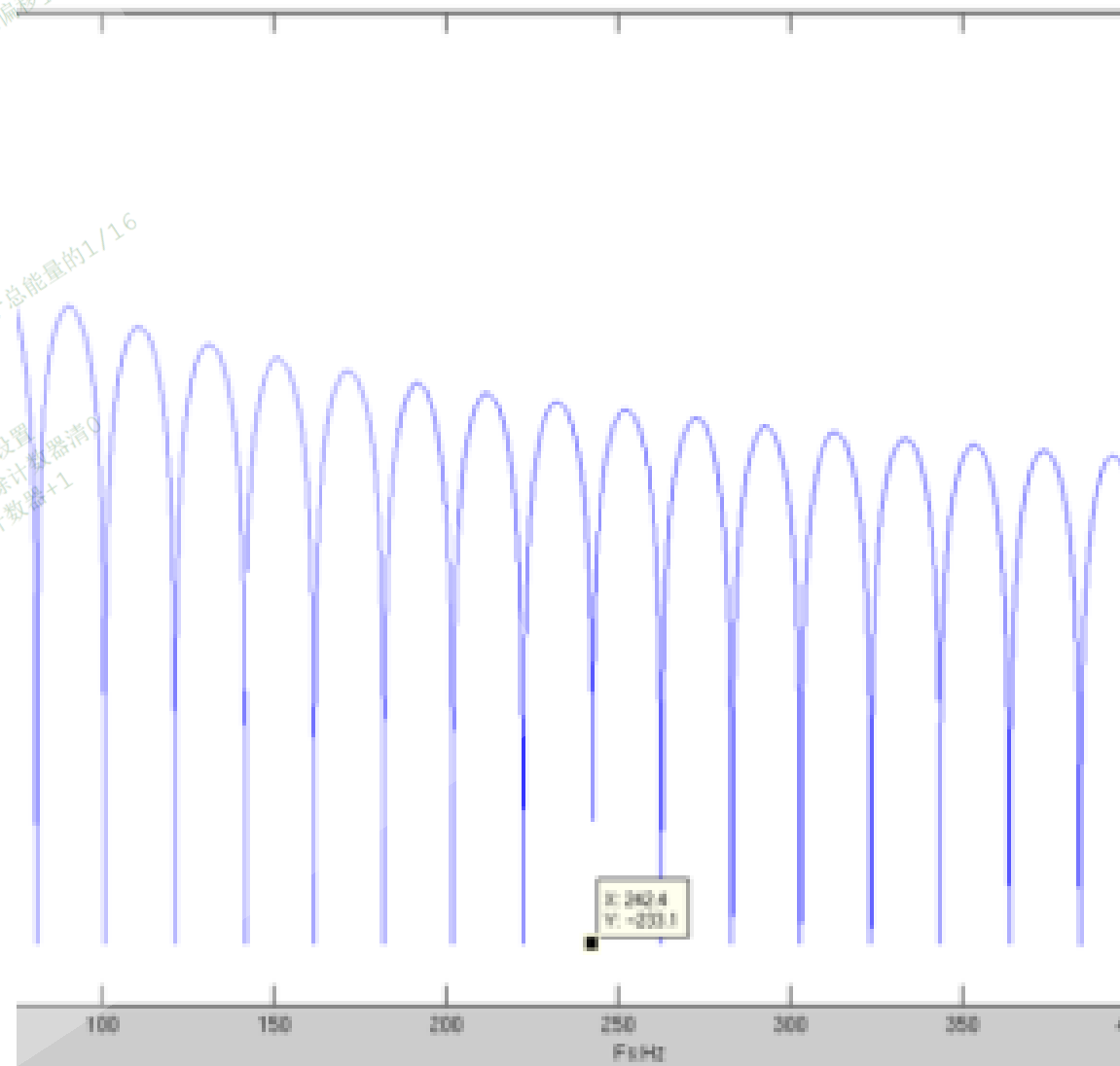
灵活可配置的多通道压缩系统

- 基于配置文件的多通道划分
- 快慢时间侦测器
- 灵活的时间常数配置
 - 噪音环境使用慢压缩
 - 安静环境使用快压缩



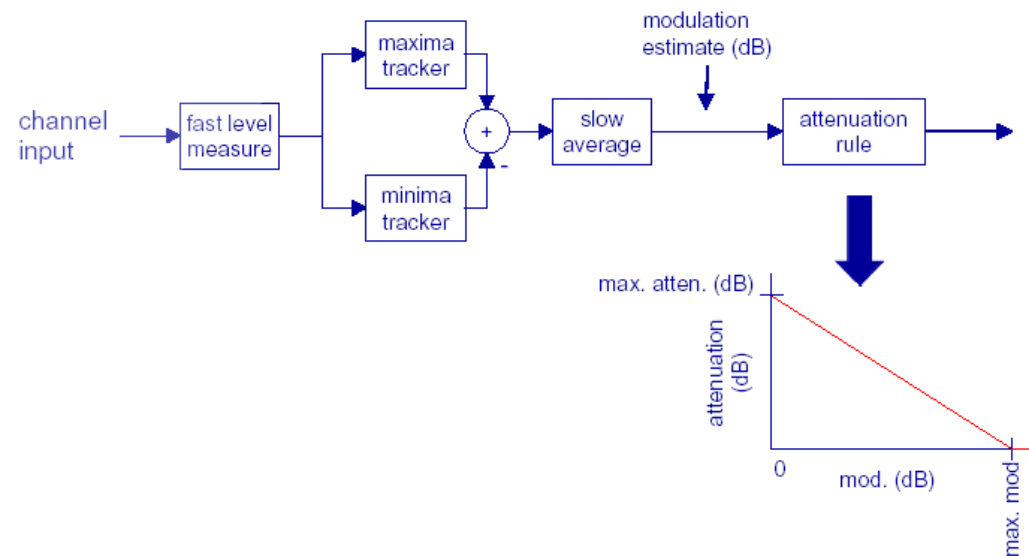
通道反馈侦测抑制处理

- 自适应陷波滤波器
 - 通道能量统计
 - 找出峰值能量通道
 - 峰值通道能量与总能量比较
 - 计算反馈指数
 - 根据反馈指数决定是衰减通道增益还是恢复通道增益



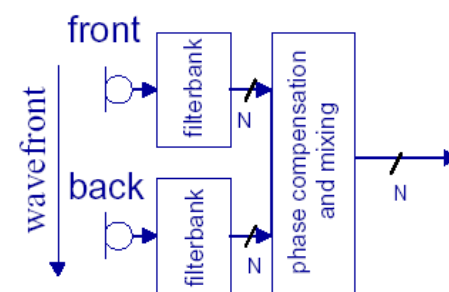
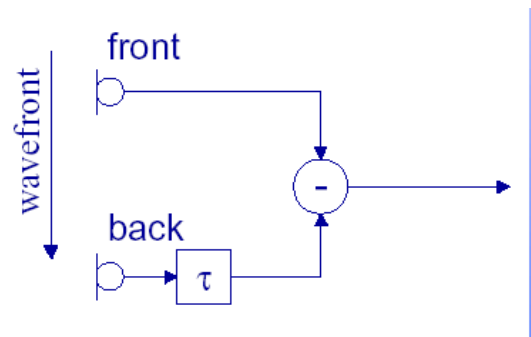
基于短时频谱分析的智能降噪算法

- 通道信号变化分析
- 统计通道能量变化量率
- 根据通道变化率计算噪音指数



方向性处理

- 2个麦克风输入
- 根据前后声音能量大小估计噪音方向
- 自动计算延时常数 τ 改变方向性指数



其它功能

- 提示音系统Beep system
- 多程序配置Multi-memoriy
- 低电量警报Low battery alear
- 原位测听In-suit audiometry
- 数据日志Data logging

END

- 参考资料Ref.
 - BelaSigna®300 [\[官方链接\]](#)
 - *Hearing Aids* by Harvey Dillon [\[购买链接\]](#)
 - *Digital Hearing Aids* by James M. Kates [\[购买链接\]](#)
 - *Computer Architecture: A Quantitative Approach* by Hennessy, John L., and Patterson, David A. [\[购买链接\]](#)
- 参考手册
 - *Integrated Development Environment User's Guide*
 - *CFX DSP Architecture Manual*
 - *Hardware Reference Manual for Ezairo 5900*
 - *Firmware Reference Manual*
 - *HEAR Configurable Accelerator Reference Manual*
 - *CFX Toolchain Reference*

